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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/828,592

04/21/2004

Betty Shu Mercer

TI 36275

5550

23494

7590

04/16/2007

TEXAS INSTRUMENTS INCORPORATED

P O BOX 655474, M/S 3999

DALLAS, TX 75265

EXAMINER

FULK, STEVEN J

ART UNIT

PAPER NUMBER

2891

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

04/16/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.		Applicant(s)	
	10/828,592		MERCER ET AL.	
	Examiner		Art Unit	
	Steven J. Fulk		2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 11-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 16-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 5-7, 9, 10, 16-17, 19-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang '878 in view of Harris '382.

- a. Regarding claims 1 and 16, Wang discloses a method for manufacturing an integrated circuit comprising forming transistor devices over a semiconductor substrate (fig. 1, 10; col. 5, lines 15-25); forming one or more metallization layers over the transistor devices, the one or more metallization layers interconnecting one or more of the transistor devices (col. 4, line 66 – col. 5, line 14); forming a protective overcoat (fig. 1, 14a/14b) over the one or more metallization layers, wherein the protective overcoat has an opening located therein (fig. 1; opening in layer 14 to layer 12); forming a surface conductive lead (fig. 2, 20) in the opening and over a barrier layer (16a), a portion of the barrier layer extending beyond the surface conductive lead (col. 8, line 42 – col. 9, line 51; electrode 20 is formed and then barrier layer 16 is etched); and subjecting the portion of the barrier layer to a dry etch to remove the portion, the dry etch selective to the barrier layer (col. 9, lines 39 – 51; barrier layer is dry etched with a

conventional dry etch method such that negligible thickness of electrode 20 is lost).

Wang does not explicitly disclose forming a skirt when subjecting the portion of the barrier layer to a dry etch. Harris teaches a method for manufacturing an interconnect for an integrated circuit comprising forming a surface conductive lead (fig. 4, 28a) in an opening of formed within a protective overcoat (24) and over a barrier layer (28b), a portion of the barrier layer extending beyond the surface conductive lead to form a skirt (36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the barrier layer skirt of Harris in the method for manufacturing an integrated circuit of Wang. One would have been motivated to do this because forming the barrier layer skirt under the surface conductive lead would have widened the base of the surface conductive lead and reduced the stress on the protective overcoat layer that occurs during packaging of the integrated circuit (Harris, col. 3, lines 21-28), thus reducing the risk of cracking of the overcoat layer and improving the device performance (Harris, col. 2, lines 41-57).

b. Regarding claim 5, Wang in view of Harris teaches all of the elements of the claim as set forth in paragraph 4a, and Wang also discloses the barrier layer to be tungsten titanium (col. 6, lines 50-53).

c. Regarding claim 6, Wang in view of Harris teaches all of the elements of the claim as set forth in paragraph 4a, and Wang also discloses the barrier

layer to have a thickness ranging from 200 nm to 300nm (col. 6, lines 59-65).

d. Regarding claims 7 and 17, Wang in view of Harris teaches all of the elements of the claims as set forth in paragraph 4a, and Wang also discloses a seed layer located between the barrier layer and the surface conductive lead (fig. 5, 17), wherein the seed layer comprises copper; and further including subjecting the seed layer to a wet etch (col. 11, line 59 – col. 12, line 4) prior to subjecting the portion of the barrier layer to the dry etch.

e. Regarding claims 9 and 19, Wang in view of Harris teaches all of the elements of the claims as set forth in paragraph 4a, and Wang also discloses the surface conductive lead to have a width ranging from 3 μm to 200 μm (col. 5, lines 41-47).

f. Regarding claims 10 and 20, Wang in view of Harris teaches all of the elements of the claims as set forth in paragraph 4a, and Wang also discloses the protective overcoat to comprise silicon oxynitride layers, silicon oxide layers, and silicon nitride layers (col. 6, lines 5-24).

3. Claims 2-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang '878 in view of Harris '382, and further in view of Ashby et al. '238.

Wang in view of Harris teaches all of the elements of the claims as set forth in paragraph 4a, including the disclosure by Wang of using a dry etch to remove portions of the barrier layer, but the references do not explicitly disclose the use of carbon tetrafluoride and nitrous oxide, oxygen or chlorine as the dry etch chemistry. Ashby et al. teaches a method of etching tungsten titanium alloys (col.

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4, lines 2-6) using a dry etch chemistry of carbon tetrafluoride and nitrous oxide, oxygen or chlorine (col. 4, lines 58-65; col. 6, lines 29-47) in the fabrication of integrated circuits (col. 4, lines 31-42).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the dry etch chemistry of Ashby et al. in the method for manufacturing an interconnect as described by Wang in view of Harris. One would have been motivated to do this because Wang taught that it was desirable to use a conventional dry etch that was selective to the barrier layer to remove portions of it (Wang, col. 9, lines 39-51), and Ashby et al. taught that a dry etch chemistry of carbon tetrafluoride and nitrous oxide, oxygen or chlorine was well known to be highly selective to the tungsten titanium alloy, thus removing the barrier layer without damaging the surrounding layers of the device (Ashby et al., col. 2, lines 40-52).

4. Claims 8 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Wang '878 in view of Harris '382, and further in view of Backus '124.

Wang in view of Harris teaches all of the elements of the claims as set forth in paragraph 4a and 4d, including the disclosure by Wang of using a wet etch to remove portions of the copper seed layer, but the references do not explicitly disclose the wet etch chemistry to include hydrogen peroxide and sulfuric acid. Backus teaches a method of etching copper in fabricated printed circuits (col. 1, lines 5-11) using a wet etch chemistry including hydrogen peroxide and sulfuric acid (col. 2, lines 43-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the wet etch chemistry of Backus in the method for manufacturing an interconnect as described by Wang in view of Harris. One would have been motivated to do this because Wang taught that it was desirable to use a conventional wet etch to remove portions of the seed layer (Wang, col. 9, lines 39-51), and Backus taught that a wet etch chemistry including hydrogen peroxide and sulfuric acid was a well known chemistry used to etch copper that also prevented cementation of copper onto other metal surfaces during etching, thus providing a clean surface conductive lead for subsequent wire-bonding and packaging steps.

Response to Arguments

5. Applicant's arguments with respect to independent claims 1 and 16 have been considered but are not found persuasive.

Applicant argues that Harris does not teach metal layer 28b to be a barrier layer. This argument is not found persuasive because claims 1 and 16 are written broadly enough to be anticipated by any layer under a surface conductive lead that prevents direct contact and diffusion of materials with an underlying bond pad, thus acting as a barrier layer. In this case, the layer 28b of Harris is a barrier between bond pad 26 and surface conductive lead 28.

Applicant also argues that Harris teaches reducing the base of the surface conductive lead, citing a base reduction from fig. 2 to fig. 4, as opposed to widening it with a skirt. This argument is not found persuasive because Harris is teaching a widening of the bond pad from fig. 2, element 14 to fig. 4, element 26. The surface conductive lead retains a skirt in both embodiments. Harris teaches that the

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underlying layers should be wider than upper layers to reduce stress of the bonding process (col. 2, lines 41-45; force applied during bonding) and prevent cracking of the interlayer dielectrics (col. 1, lines 38-48; oxide cracking from surface conductive bump lead being wider than bond pad; col. 3, lines 14-20; expand bond pad to exceed area of lower surface of conductive bump). Therefore, Harris teaches in general that expanding underlying layers to a width greater than upper layers reduces the stress the layers are subjected to during bonding and prevents cracking. The bond pad 26 is wider than the skirt in layer 28b, and the skirt is wider than upper bump lead 28. Therefore, one of ordinary skill in the art would have been motivated to form the barrier layer skirt of Harris in the method for manufacturing an integrated circuit of Wang in order to reduce the stress on the protective overcoat layer that occurs during packaging of the integrated circuit, as set forth above.

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will

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the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven J. Fulk
Patent Examiner
Art Unit 2891
April 11, 2007

SJF


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